The solder paste printing process: critical parameters, defect scenarios, specifications, and cost reduction

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Abstract

Purpose – The purpose of this paper is to comprehensively explore the effects of critical parameters on solder deposition and to establish a systematic approach for determining guidelines for solder paste inspection (SPI) workstations.

Design/methodology/approach – This study explored the effects of process parameters, stencil and printed circuit board designs on solder deposition and identified the major post-reflow defect scenarios. Through the investigation of correlation between the results of SPI analysis and post-reflow defective scenarios, SPI specifications are suggested for minimizing the total cost of poor quality.

Findings – The higher the printing pressure the lower the solder deposition. There was a significant difference in solder deposition between the front squeegee and the rear squeegee. Insufficient distance between the stencil aperture and the initial printing location resulted in irregular solder paste and variations in solder deposition. A stencil with a higher area ratio resulted in greater solder deposition and less variation. Stencil apertures parallel to the direction of printing were superior to a 45° vector print. Further, the nominal solder thickness should take into account the thicknesses of the solder mask and the legend ink. There was an offset in the results of SPI measurements between the solder mask defined (SMD) pads and non-SMD pads. The specifications for solder deposition with irregular stencil apertures need to be adjusted.

Originality/value – To address the arbitrariness of existing industry practice, this study was a joint effort with a Taiwan-based electronics manufacturing service company. Real data were taken from a mass production environment and inferences were then made based on a statistical analysis.

Keywords Printing process, Stencil, Solder paste inspection, Post-reflow defects, SPI specifications, Cost of poor quality, Solder mask, Printing industry, Solder paste

Paper type Research paper

1. Introduction

Miniaturization and high functionality are critical trends in the semiconductor packaging industries. Engineering teams encounter the challenges of increased functional density and reduced input/output (I/O) spacing (Wang *et al.*, 2007; Durairaj *et al.*, 2001; Huang *et al.*, 2009). In the printed circuit assembly process with surface mount technology, solder paste consisting of solder particles and flux is deposited onto the printed circuit board (PCB) bonding pads using stencil printing. The electronic components are then placed onto the PCB by a pick-and-placement machine. During reflow soldering, the solder paste melts and solidifies to form reliable solder joints. Industry reports indicate that approximately 50-70 per cent of soldering defects are attributable to the solder paste printing process (Pan *et al.*, 2004; Tsai, 2008; Huang, 2004). Thus, for the desired process yield and reliable interconnections, variations in the solder paste deposition should be minimized.

Researchers have investigated the printing performance of different solder paste materials, PCB pad designs, stencil aperture designs and printing process parameters (Arra *et al.*, 2004; Ladani *et al.*, 2008). An and Wu (2010) developed a print tester that measured the characteristics of the squeegee/stencil interaction to monitor the printability of solder paste. Greene and Srihari (2008) determined how fast a selection of lead-free pastes could be successfully printed. Mannan *et al.* (1994) and Pan (2000) reported that stencil aperture design significantly influenced the ability to achieve appropriate paste volume. Pan *et al.* (2004) examined the effects of aperture size, aperture shape, board finish, stencil thickness, solder type and print speed. These findings are useful for understanding the various process issues involved in assembly yield and the factors that affect it. However, the inferences made from these studies are based on a limited quantity of experimental data. Nevertheless, stencil printing still exhibits sophisticated characteristics owing to the nature of the process and unavoidable random variations, especially in the mass production environment.

While an excessive amount of solder paste deposition may cause solder bridging (electrical shorts), insufficient solder will result in unreliable solder joints or electrical opens.

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Hence, after the printing process, a solder paste inspection (SPI) system is generally used to examine the solder paste deposition (Figure 1) (Huang, 2010). SPI inspection refers to the three-dimensional (3D) measurement of solder thickness, area, volume and regularity of the solder deposition through laser-based scanning technology. The template frame is used to determine the area of solder deposition (Figure 1). An SPI system is capable of examining solder deposition to identify both systematic and random printing errors before boards are sent for subsequent component placement (Tsai, 2008). After programming for the locations of the bonding pads on the PCB, automatic online inspection is carried out. Defective boards with inappropriate solder printing are screened for rework (Durairaj *et al.*, 2008; Greene and Srihari, 2008; Barajas *et al.*, 2008). This continuous, real-time feedback was expected to improve the process yield.

Currently, the inspection criterion for solder thickness used in the electronics assembly industry is determined subjectively, with a certain percentage of the stencil thickness, such as ±70 per cent. A review of the literature indicates that there is little research on the determination of reasonable inspection criteria. Huang (2010) defined the specifications for distinguishing acceptable PCB samples from defective ones. In his study, the Mahalanobis distance of the solder thickness from the verification samples was compared to the threshold. This was to confirm if the model was capable of differentiating normal/abnormal PCB samples (Huang, 2010). However, while solder printing is only an intermediate process in electronics assembly, decisive defects occur only after the reflow soldering. Therefore, an effective determination of the SPI criterion should be based on the occurrence of post-reflow defects, defects observed during the automatic optical inspection (AOI) stage after reflow soldering.

2. Research objective and methodology

To address the arbitrariness of existing industry practice, this study was a joint effort with a Taiwan-based electronics manufacturing service company. Real data were taken from a mass production environment and inferences were then made based on a statistical analysis. The objective was to comprehensively explore the effects of critical parameters on solder deposition and to establish a systematic approach for determining guidelines for SPI workstations in electronics manufacturing environments.

This study utilized experimental design to explore the effects of process parameters, stencil apertures and PCB designs on solder deposition and to identify the major post-reflow defect scenarios. The Weibull probability distribution was used to describe the occurrence of defects. Through the investigation of correlation between the results of SPI analysis and post-reflow defective scenarios, the SPI specifications are suggested by minimizing the total cost of poor quality (CoPQ).

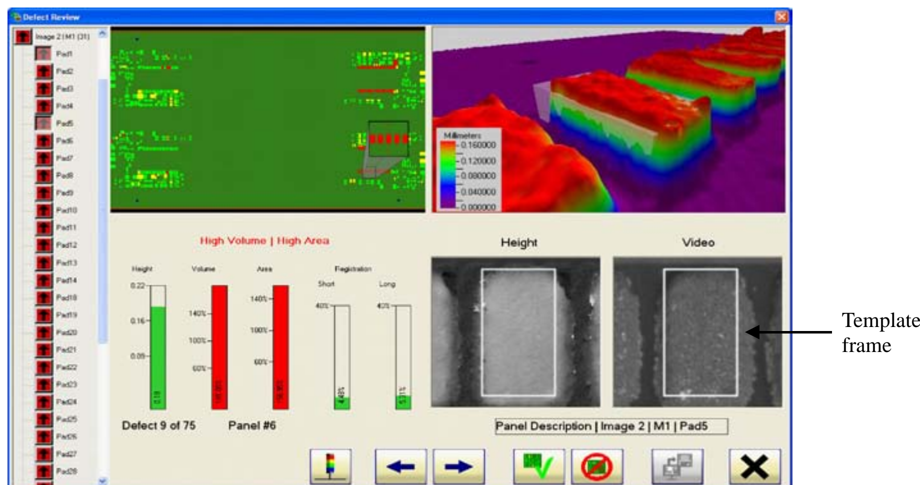
3. The effects of process parameters, stencil and PCB designs on transfer ratio during solder paste deposition

Solder paste printing is complex, with many interactions between influential factors, and it exhibits nonlinear characteristics owing to the nature of the process and unavoidable random variations (Tsai, 2008). This study investigated the data collected from the production environment and determined the critical factors that influenced the solder paste deposition. The transfer ratio of the solder thickness, the solder area and the solder volume are defined as the ratio of the stencil features (stencil thickness, stencil aperture size, stencil aperture volume) to the actual solder paste deposition (solder paste thickness, solder paste area, solder volume). The coefficient of variations (CV) is defined as the standard deviation (of solder paste thickness, area or volume) divided by its average.

3.1 Printing process parameters

The critical process parameters that influence the printing quality were investigated. Factors considered include printing pressure, front/rear squeegee and the distances from the stencil aperture to the initial printing location and to the board edge. The deposition of solder paste for 0402 passive components was measured on a server product in the manufacturing facility.

Figure 1 Solder paste inspection



3.1.1 Printing pressure

The thickness (mm) of solder deposition using printing pressures of 7.4 and 8.4 kg was evaluated for pads at six regions on the board. The results showed that a higher printing pressure resulted in a lower amount of solder deposition with respect to the solder thickness (Table I and Figure 2). This is because solder paste is scooped away if excessive pressure is applied during printing.

3.1.2 Front/rear squeegee

The stencil printing machine used in this study had two squeegees, one for the forward stroke and the other for the reverse stroke. Odd-numbered boards were printed with the front squeegee and even numbered with the rear squeegee. The solder depositions resulting from the two squeegees (front and rear) were compared. A printing pressure of 8.2 kg was used. Table II and Figure 3 show the thickness (mm) of solder depositions at three regions on the boards. The results show that the amount of solder deposition by the rear squeegee was significantly larger than from the front squeegee. This phenomenon also occurred with other models of products made in the manufacturing facility. Figure 4 shows the configurations of the fixtures of the front squeegee and the rear squeegee. It is apparent that the rod applying printing pressure was not properly aligned on top of the fixture (squeegee) for the rear squeegee. Therefore, the pressure applied to the rear squeegee during the printing process was lower than the set print pressure. In this case, the reverse scooping phenomenon occurred: a lower printing pressure resulted in a larger amount of solder deposition due to the absence of scooping.

Table I Solder deposit thickness using printing pressures of 7.4 and 8.4 kg

Printing pressure	8.4 kg Average	8.4 kg SD	8.4 kg Sample size	7.4 kg Average	7.4 kg SD	7.4 kg Sample size
Region 1	0.1361	0.0044	20	0.1423	0.0034	20
Region 2	0.1329	0.0034	20	0.1744	0.0115	20
Region 3	0.1323	0.0035	20	0.1714	0.0055	20
Region 4	0.1351	0.0035	20	0.1743	0.0055	20
Region 5	0.1347	0.0046	28	0.1390	0.0056	28
Region 6	0.1352	0.0033	20	0.1440	0.0043	20

3.1.3 Distances to the initial printing location

The solder depositions from both the front and rear squeegees were evaluated to investigate the influence of the distances of the stencil aperture to the initial printing location. The thickness (mm) of the solder depositions on the two regions (regions A and B) was measured (Figure 5). As shown in Table III and Figure 6, a more severe variation in solder deposition at region B appeared if the front squeegee was used. By the same token, more severe variations in solder deposition were observed at region A if the rear squeegee was used. Region A (region B) was less distant from the initial print location if the front squeegee (rear squeegee) was used. This was because during the printing process, the solder paste was rolling and became smooth and uniform during its travel in front of the squeegee (Figure 7). The smoothness of the rolled solder paste depended on how far it travelled on the stencil. An insufficient distance from the stencil aperture to the initial printing location resulted in irregular solder paste and thus more severe variation in solder deposition.

Figure 2 Effects of printing pressure on the solder deposition at various regions

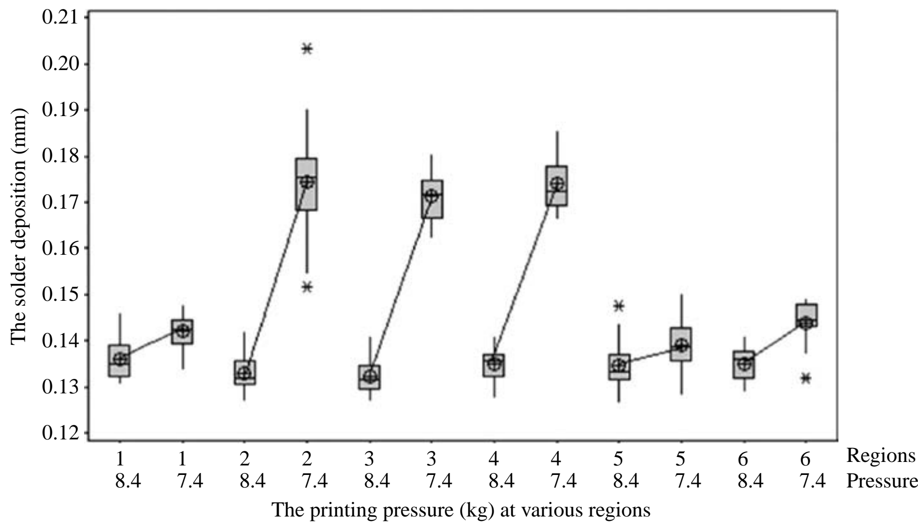


Table II Solder deposition thickness resulting from the front squeegee and the rear squeegee

	Rear squeegee Average	Rear squeegee SD	Rear squeegee Sample size	Front squeegee Average	Front squeegee SD	Front squeegee Sample size
Region 1	0.1349	0.0041	20	0.1302	0.0028	20
Region 2	0.1362	0.0052	18	0.1688	0.0047	18
Region 3	0.1351	0.0041	20	0.1649	0.0065	20

Figure 3 The effects of front/rear squeegee on the solder deposition

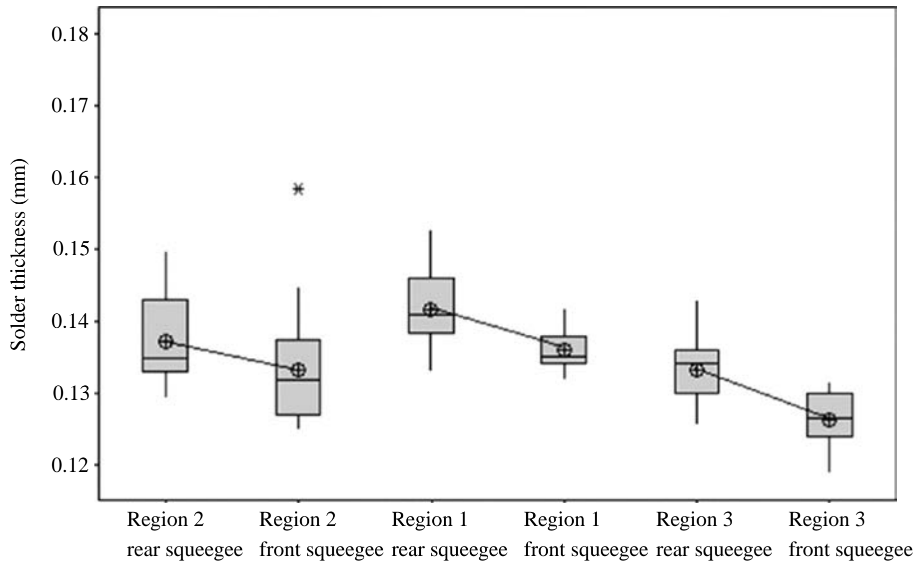
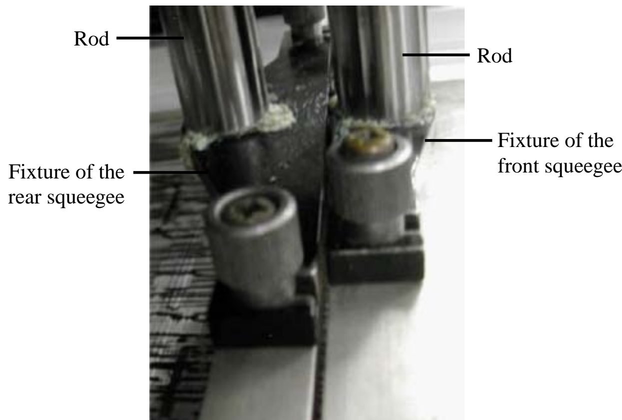


Figure 4 Configuration of fixtures on the front and rear squeegees



3.1.4 Distances to the board edge

To further assess variation in solder deposition across the PCB, a total of ten sample boards were printed consecutively. Odd-numbered boards were printed with the front squeegee, even-numbered with the rear squeegee. The boards were 433 mm in length and 242 mm in width. The entire board was divided into 11 regions of 22 mm in width (as shown in Figure 5). For each region, solder depositions on a total of 30 bonding pads were measured. Figure 8 shows the average solder deposition (thickness in mm) across the 11 regions for the ten boards. Results show that the solder thickness in regions numbers 1 and 11 (near the edge of the board) were significantly higher than in the other regions. This was due to a gap between the stencil and the board surface at the board edge that results from the presence of the fixture that secures the PCB on the conveyor (as shown in Figure 9).

Figure 5 The PCB to be measured for the solder deposition

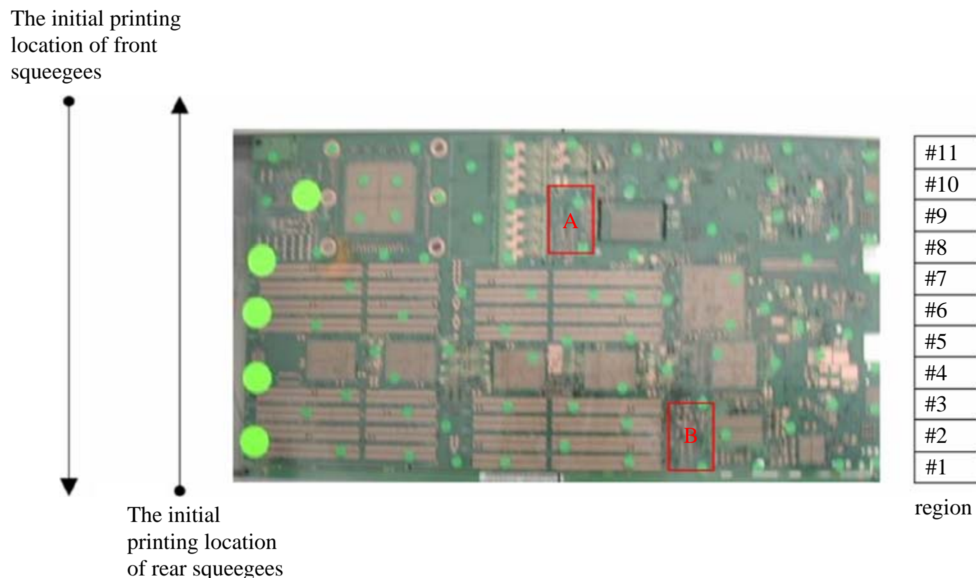


Table III The thickness of solder depositions with different distances of the stencil aperture to the initial printing location

	Rear squeegee			Front squeegee		
	Average	SD	Sample size	Average	SD	Sample size
Region A	0.1481	0.0141	16	0.1534	0.0077	16
Region B	0.1383	0.0090	16	0.1549	0.0110	16

Figure 6 Effect of distance from the stencil aperture to the initial printing location

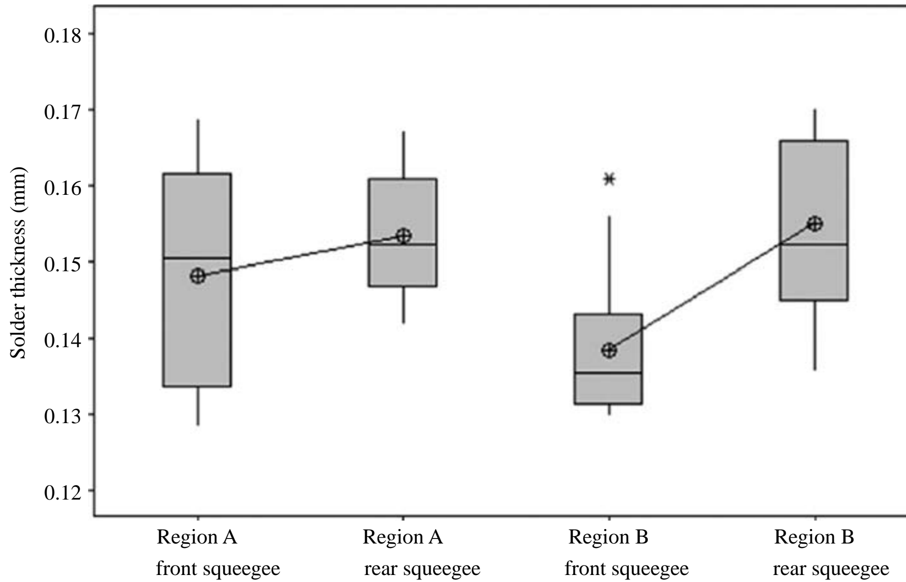
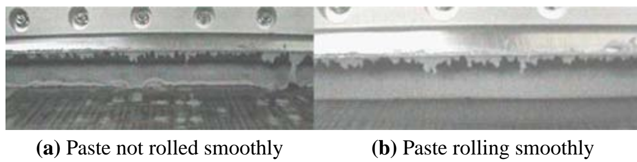


Figure 7 Solder paste rolling outcomes



(a) Paste not rolled smoothly **(b)** Paste rolling smoothly

Figure 8 Solder depositions across the 11 regions of the sample boards

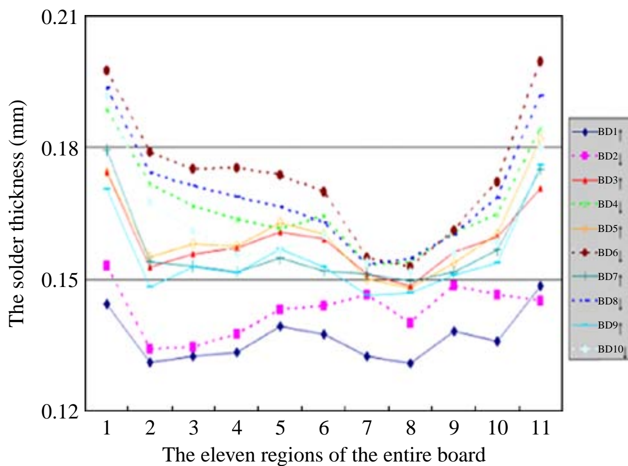
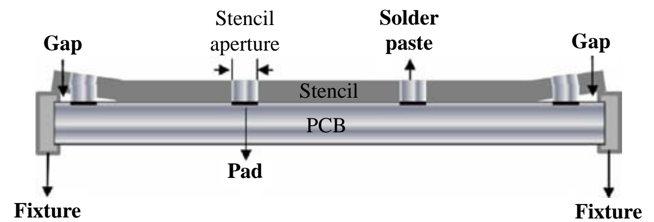


Figure 9 Gap between the stencil and the board surface at the board edge



Consequently, an additional amount of solder was deposited on the bonding pads at regions near the board edge.

Results also show that the solder depositions on the first and second boards were significantly lower than on the other boards, because air blisters in the newly supplied solder paste caused irregularities on the paste surface. Therefore, a test printing of at least two boards is essential at the beginning of mass production.

In addition, the results again confirmed that the solder deposition of the rear squeegee (Figure 8, dotted line) was significantly greater than from the front squeegee (Figure 8, solid line).

3.2 Stencil design parameters

The stencil design plays an important role in the deposition of solder paste during the printing process. The occurrence of stencil thickness variation and influences of aperture features are investigated in this section.

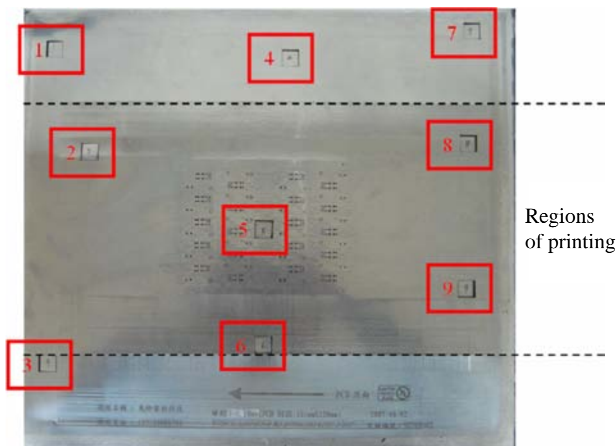
3.2.1 Variation in stencil thickness

Variation in stencil thickness occurs in the stencil manufacturing process and results in the variability of solder deposition. The amount of variation depends on the nominal (designed) stencil thickness. This study evaluated stencils with thicknesses of 0.12 and 0.10 mm and nine regions in the stencil samples, each with a size of 15 mm × 15 mm, were considered (Figure 10). Each stencil coupon (region) was measured for its thickness at three locations through cross-sectional analysis. While the industry standard indicates that the stencil manufacturing tolerance is ±0.005 mm, the specifications for the 0.12- and 0.10-mm stencils were in the ranges of 0.115-0.125 and 0.095-0.105 mm, respectively. For the 0.12-mm stencil, the results showed that three out of the 27 readings exceeded the specification (Table IV). Out of 27 readings, eight exceeded the specification for the 0.10-mm stencil. However, there was no significant difference from a statistical point of view. In addition, stencil thickness variation can also occur as a result of wearing during the printing process. Results (from the 0.12-mm stencil) showed that several printing regions (2, 5, 6, 8 and 9) exhibited lower thickness.

3.2.2 Directions of stencil aperture

The stencil aperture is typically based on the dimensions of the pad designs. For rectangular bonding pads (for components such as quad flat package (QFP) or SOIC), the stencil apertures are usually either parallel or vertical to the direction of stencil printing. Nevertheless, a special design may have a 45° vector print. For 45° aperture designs, the squeegee is in contact with the sharp corner of the stencil aperture, which may impact the solder deposition. In this study, stencil apertures (with dimensions of 0.67 mm × 0.60 mm) were oriented to 0 and 45° with respect to the direction of printing. The resulting transfer ratios (ratio of solder thickness to the stencil thickness) are shown in Table V and Figure 11. The transfer ratio on bonding pads of 45° printing was significantly less than that of 0° printing. The sharp corner appeared to impede the transfer of solder paste during the printing process.

Figure 10 Regions of the 0.12-mm stencil under evaluation



3.2.3 Aspect ratio and area ratio of stencil aperture design

The aspect ratio is defined as the ratio of aperture width to the stencil thickness, while the area ratio is defined as the ratio of aperture area to the area of aperture wall surface. Industry standard IPC 7525 specifies that, for effective printing, the aspect ratio and area ratio of a stencil design should be greater than 1.5 and 0.66, respectively. Practical data of solder transfer ratio using different stencil designs (aspect ratio and area ratio) were collected from the manufacturing line. It should be noted that, in addition to the different stencil designs, data were also taken from various printing process parameter settings. Figure 12 shows that solder transfer ratio (with respect to the area) increased with larger aspect ratio (and area ratio) designs. The CV in solder transfer ratio decreased with larger aspect ratio designs. This is because the solder paste tended to adhere to the stencil aperture wall during the release of the stencil from the board. This scenario was more severe for applications with a smaller aspect ratio (and area ratio). Finally, while the trend showing the correlation between solder transfer ratio and stencil aspect ratio design does exist (Figure 12), the fluctuation of the data is due to the fact that data were collected from various printing process parameter settings as mentioned above.

3.3 PCB design parameters

In this section, the solder mask thickness was measured and the results compared to the industrial standard. Further, the influence of bonding pad definition methods on the SPI measuring result (solder thickness) is explored.

3.3.1 Solder mask thickness

The surface of a PCB is typically covered by solder mask and legend ink to prevent solder bridging and to denote the location of components. Typical specifications for solder mask

Table IV The thicknesses of the stencils at various regions

	0.12 mm			0.10 mm		
	Location 1	Location 2	Location 3	Location 1	Location 2	Location 3
No.1	0.1214	0.1218	0.1216	0.0950[a]	0.0910[a]	0.0938[a]
No.2[b]	0.1223	0.1211	0.1223	0.0955	0.0950[a]	0.0953
No.3	0.1204	0.1205	0.1214	0.0958	0.0941[a]	0.0938[a]
No.4	0.1229	0.1225	0.1238	0.0967	0.0970	0.0943[a]
No.5[b]	0.1247	0.1205	0.1185	0.0954	0.0952	0.0965
No.6[b]	0.1162	0.1122[a]	0.116	0.0967	0.0968	0.0963
No.7	0.1213	0.1215	0.1206	0.0977	0.0965	0.0979
No.8[b]	0.1185	0.1172	0.1174	0.0972	0.0996	0.0975
No.9[b]	0.1143[a]	0.1151	0.1149[a]	0.0942[a]	0.0962	0.0965

Notes: [a]Regions with thickness out of specification; [b]regions worn-out by the squeegee during the printing process

Table V The resulting transfer ratios on bonding pads of 0 and 45° printing

	Rear squeegee			Front squeegee		
	Average (%)	SD	Sample size	Average (%)	SD	Sample size
0° print	146.37	0.0836	100	147.61	0.0902	52
45° print	138.51	0.0624	96	137.71	0.0696	52

thickness are in the range of 0.007-0.017 mm and the total thickness of the solder mask and the legend ink should not exceed 0.035 mm. Measurements of 20 PCB samples taken from the production line all exceeded the 0.035 mm specification and the average was 0.038 mm with a standard deviation of 0.0032 mm (Figure 13). This suggests that the nominal solder thickness during stencil printing was the thickness of the stencil plus 0.038 mm.

3.3.2 Bonding pad definition

Two methods are commonly used to determine the dimensions of the exposed bonding pads, namely solder mask defined (SMD) and the non-SMD (NSMD). SMD is when the solder mask is in contact with the bonding pad, while there is clearance between the solder mask and bonding pad for NSMD (Figure 14). In this section, the influence of pad definition methods on the SPI measurement results is explored. Figure 14 shows the pad design of a QFP component for

Figure 11 Effect of stencil aperture orientation on the transfer ratio

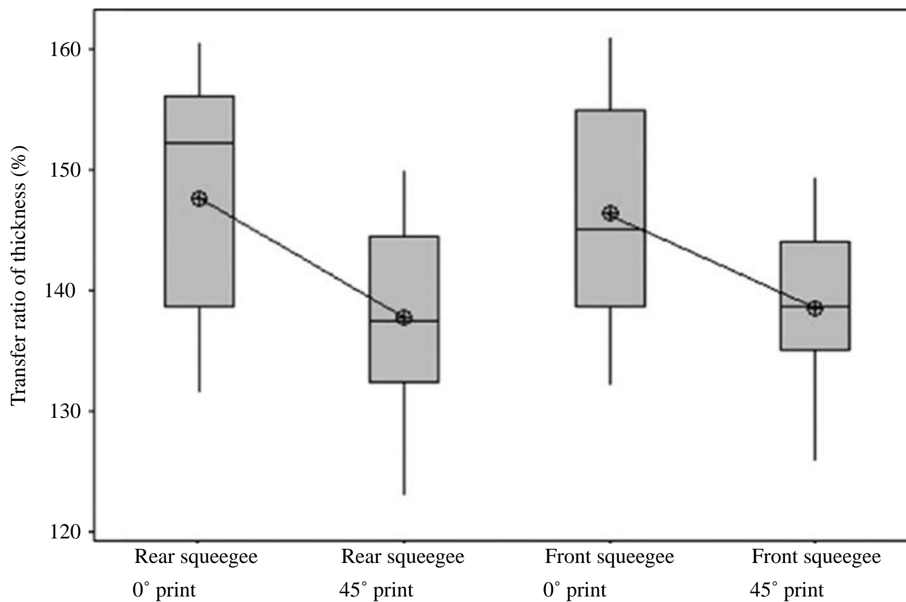


Figure 12 Correlation between solder transfer ratio and stencil aspect ratio design

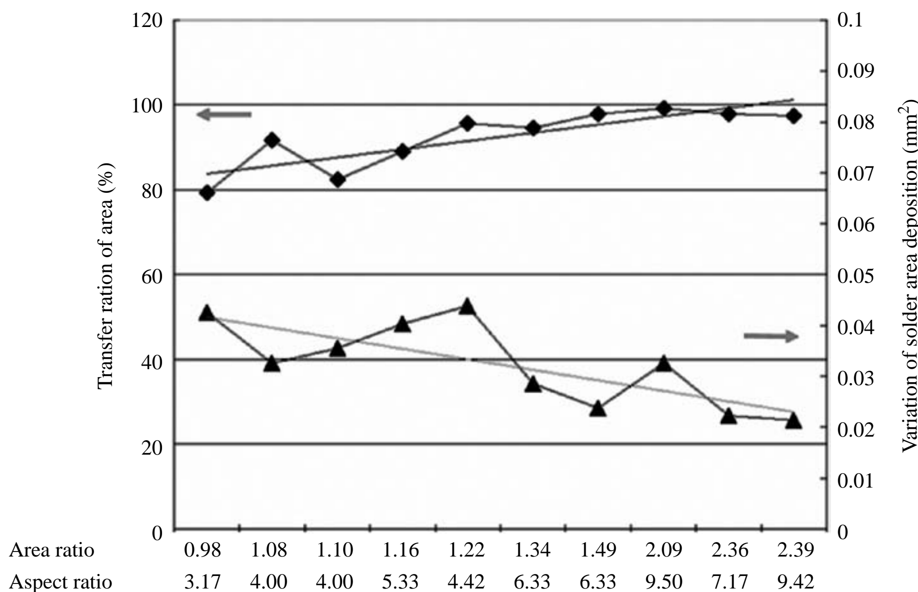
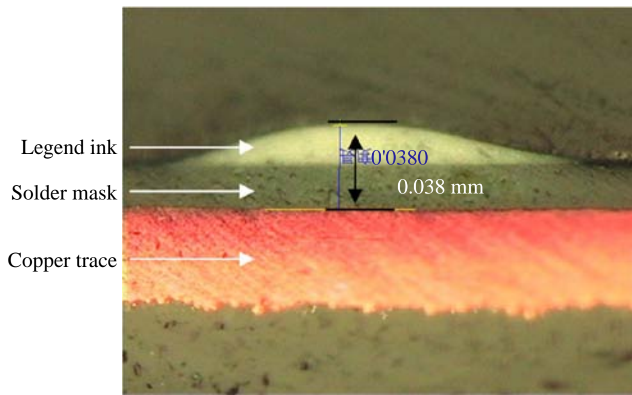


Figure 13 Total thickness of the solder mask and the legend ink



notebook computers. An SMD pad (bonding pad B) lies between the two NSMD pads (bonding pads A and C). In this case, the actual solder thicknesses are similar among the three pads. However, SPI measurement results showed that solder deposition on the SMD pads was significantly less than on the NSMD pads, by around 0.01 mm (Figure 15).

The explanation for this result is that the algorithm for the SPI apparatus was originally designed for measuring solder deposition on NSMD bond pads. A "reference scan" was performed on the bare board (without solder deposition) prior to the measurement. Figure 16 shows the frequency of different measuring heights during the reference scan. The x-axis values (height) of the first and the second peaks were used to define the heights of the PCB surface (reference plane) and the pad surface, respectively. The solder paste thickness measurement may then begin. The location of the third peak (shown in Figure 16) represents the solder paste height. The solder paste thickness was then determined by subtracting pad height from the solder paste height. For the SMD pads, as mentioned earlier, there was no clearance between the solder mask and the bonding pad. The SPI system thus incorrectly defines the first and the second peaks as the pad height and the solder mask height. The paste thickness was therefore (incorrectly) determined as paste height minus solder mask height (instead of pad height). Thus, an offset occurred in the paste thickness of the SPI measurements between the SMD pads and NSMD pads. The amount of offset is the solder mask thickness minus the pad thickness. Therefore, the SPI specification (nominal solder thickness) for SMD pads should be compensated by the above-mentioned offset.

4. The correlation between the solder deposition and occurrence of post-reflow defects

Commonly seen post-reflow defects include missing components, misaligned components, solder opens, solder shorts and tombstones. Defects that relate to the amount of solder deposition, solder opens, solder shorts and tombstones were investigated in this study. The SPI data and corresponding post-reflow defects were analyzed from a total of 37 models across product categories including servers, notebook computers and smart cards. A total of approximately 23,000 PCBs were evaluated. Figures 17 and 18 and Tables VI and VII show the correlation between the solder volume/area (in mm^3/mm^2) and the various types of post-reflow defects. The data in the figures are based on individual bonding pads. The upper part of the figures displays the occurrence of the defects and their corresponding solder volume/area. The middle parts of the figures display the distribution of solder volumes/areas on the bonding pads with location identical to the pads with occurrence of defects. The lower parts of the figures display the distribution of solder volumes/areas including all the bonding pads of the component type with occurrence of defects. These figures and tables help to show the solder volume/area of the defective bonding pads relative to that of the rest of the pads on the identical location/component.

4.1 Tombstoning

A tombstone is a defect of a passive component in which one side of the electrode is lifted and is not in contact with the bonding pad. Though solder on one side of the electrode has climbed onto the electrode, the volume of solder on the other side of electrode is insufficient to counteract the lifting of the component. This can be the result of an excessive difference in the solder volume between the two bonding pads of a passive component.

Tombstones were found on a total of ten passive components. Figure 17(a) and (b) shows the difference in solder volume (collected from SPI) between the two electrodes for a 0603 chip resistor and a LED lamp, respectively. Results show that the defective bonding pads had more significant differences in solder volume (between the two electrodes) compared to all remaining pads of the components. This indicates that tombstoning is likely to occur when the differences in solder volume reach 0.0102 and 0.02446 mm^3 for the 0603 chip resistor and LED lamp, respectively.

4.2 Solder opens

Insufficient solder is the primary cause of a solder open. A total of six bonding pads were found to have solder opens. The defective bonding pads (with occurrence of solder opens) did not appear to have lower solder volume than non-defective pads. Given this, possible causes of solder opens are poor solderability of component electrodes and inadequate lead co-planarity.

4.3 Solder shorts

Solder shorts result from:

- excessive solder volume deposition; and/or
- increased solder area due to low solder paste viscosity, causing slumping.

Figure 14 The configuration of SMD and NSMD pads

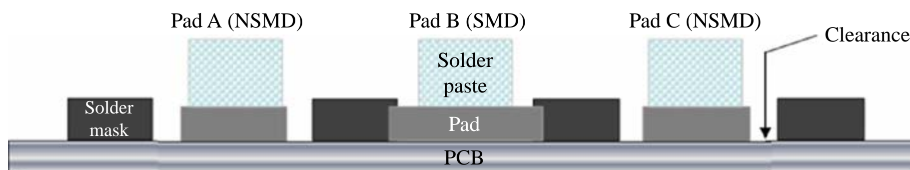
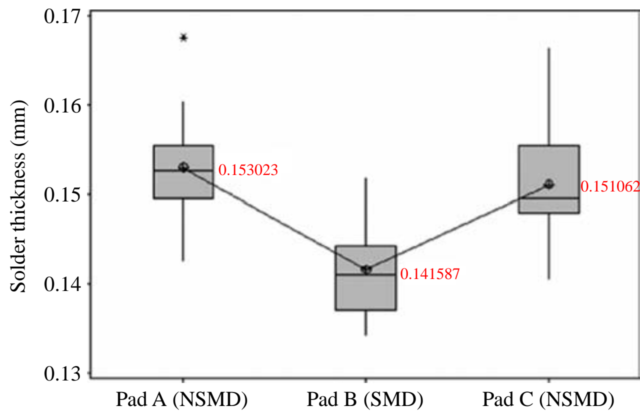


Figure 15 SPI measuring results on the SMD pads and the NSMD pads



In this section, the deposited solder volume and solder area are investigated. A total of 47 bonding pads were found to have solder shorts. Figure 18(a) and (b) shows the solder areas (collected from SPI) for 0.4-mm pitch and 0.5-mm pitch QFP components, respectively. The results show that the defective bonding pads had larger solder areas compared to all remaining pads of the components. In addition, when compared to the 0.5-mm pitch QFP components, the solder area of the 0.4-mm pitch defective QFP components was significantly less than that of the non-defective bonding pads (Figure 18). This inference is valid from both the solder volume and solder area perspectives and indicates that solder shorts are more likely to occur with fine pitch components.

5. Research on SPI specifications

The appropriateness of the SPI specifications (with respect to the solder thickness and solder area) currently used on the manufacturing shop floor for the 0402 chip components are now assessed and modifications suggested. The capability of accuracy (Ca) (equation (1)) is used as indication of the effectiveness of the specification. Further, a new SPI specification for the 0.4-mm pitch thin small outline package (TSOP) is suggested based on estimation of the CoPQ.

5.1 Adjusting the SPI specifications

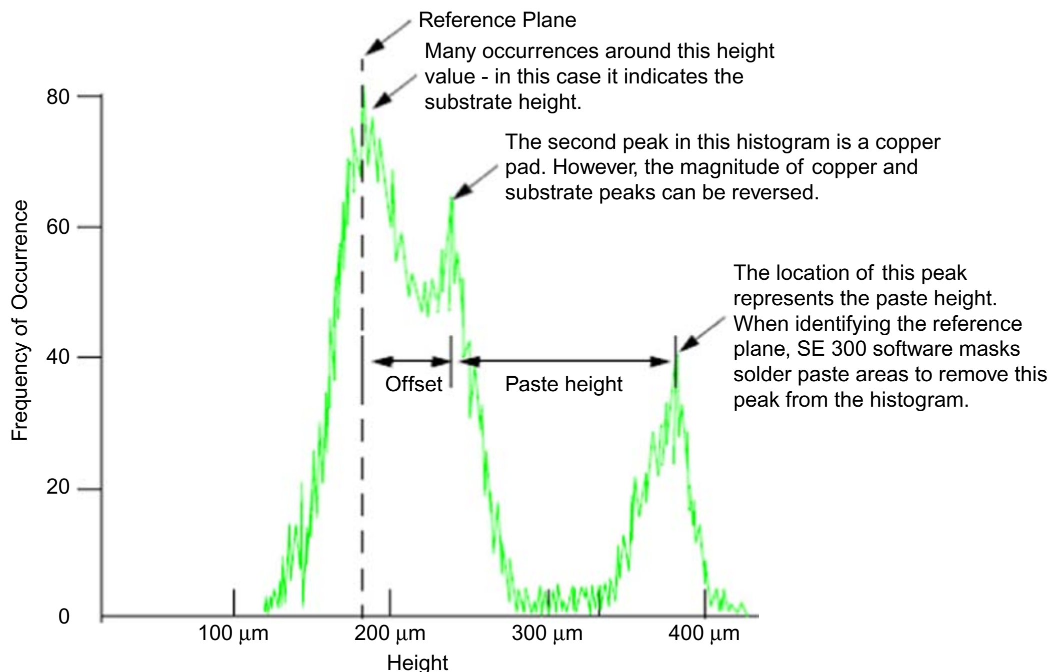
5.1.1 Solder thickness specification

As mentioned in Section 3.3.1, the presence of the solder mask and the legend ink affects the thickness of the solder deposition. The thickness of solder mask plus legend ink was found to be around 0.038 mm (Figure 13). Therefore, the SPI specification should be the stencil thickness +0.038 mm ±70 per cent. The solder depositions on both oval and rectangular bonding pads (of 0402 components) were used to verify the effectiveness of the specification. The stencil used had a thickness of 0.12 mm. Results show that the distribution of the solder thickness was well centralized at 0.158 mm, which is the sum of stencil thickness (0.12 mm) and 0.038 mm.

5.1.2 Solder area specification

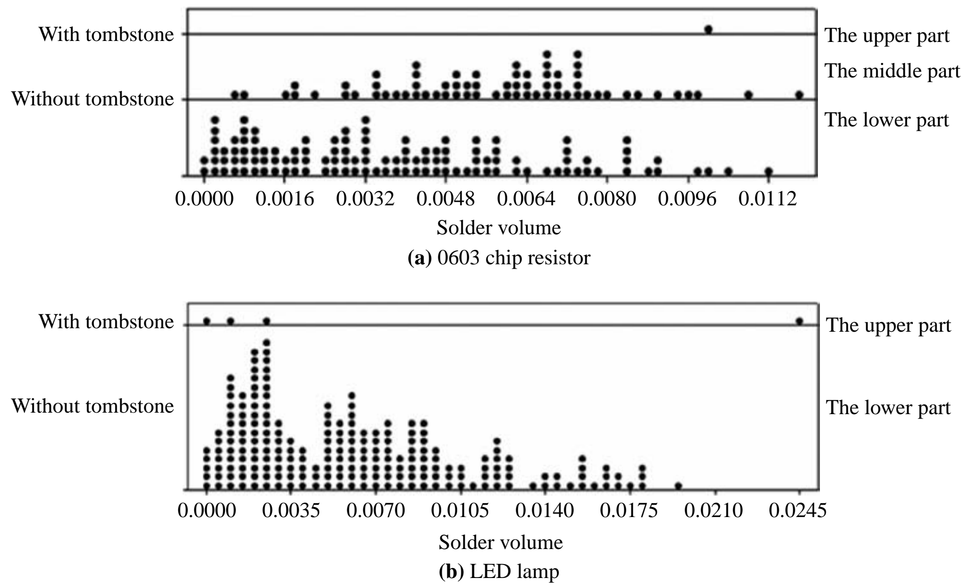
The template frame currently used for the SPI apparatus to determine the area of solder deposition is either circular or rectangular. The rectangular frame is used when the stencil aperture is "irregular" (neither circular nor rectangular). Thus, the area of the rectangular frame is considered as the nominal (target) value of the solder deposition and ±70 per cent as specification tolerance. However, in the real world, the 0402 chip components may have concave or oval pad designs (see Figure 19, which shows the distributions of solder area depositions on concave and oval pads). The distributions of these solder areas are not centralized at the specified target (Figure 19(a) and (b)). Thus, the actual area

Figure 16 Histogram of SPI measurements



Source: CyberOptics Corp.

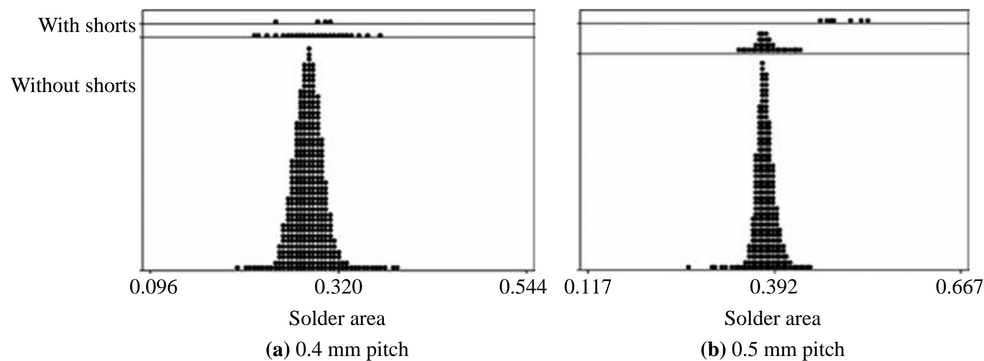
Figure 17 Differences in solder volume between the two bonding pads of a passive component



(a) 0603 chip resistor

(b) LED lamp

Figure 18 Deposition of solder area for different QFP components



(a) 0.4 mm pitch

(b) 0.5 mm pitch

Table VI The difference in solder volume between the two electrodes for 0603 chip resistors and LED lamps

	0603 chip resistor			LED lamp		
	Average	SD	Sample size	Average	SD	Sample size
Up part	0.0101	–	1	0.0073	0.0101	4
Middle part	0.0057	0.0023	67	–	–	–
Lower part	0.0038	0.0028	117	0.0058	0.0035	218

Table VII The solder area for 0.4-mm pitch QFPs and 0.5-mm pitch QFPs

	0.4-mm pitch QFP			0.5-mm pitch QFP		
	Average	SD	Sample size	Average	SD	Sample size
Up part	0.2898	0.0269	4	0.4919	0.0242	7
Middle part	0.3038	0.0136	758	0.3782	0.0121	1,526
lower part	0.2843	0.0164	65,268	0.3790	0.0132	17,360

of the stencil aperture should be calculated to define the appropriate nominal value for the inspection specification (Figure 19(c) and (d)). As a result of the adjustments for SPI specifications, the values of Ca were improved from 19.4 to 5.1 and from 50 to 24 per cent for concave and oval pads, respectively:

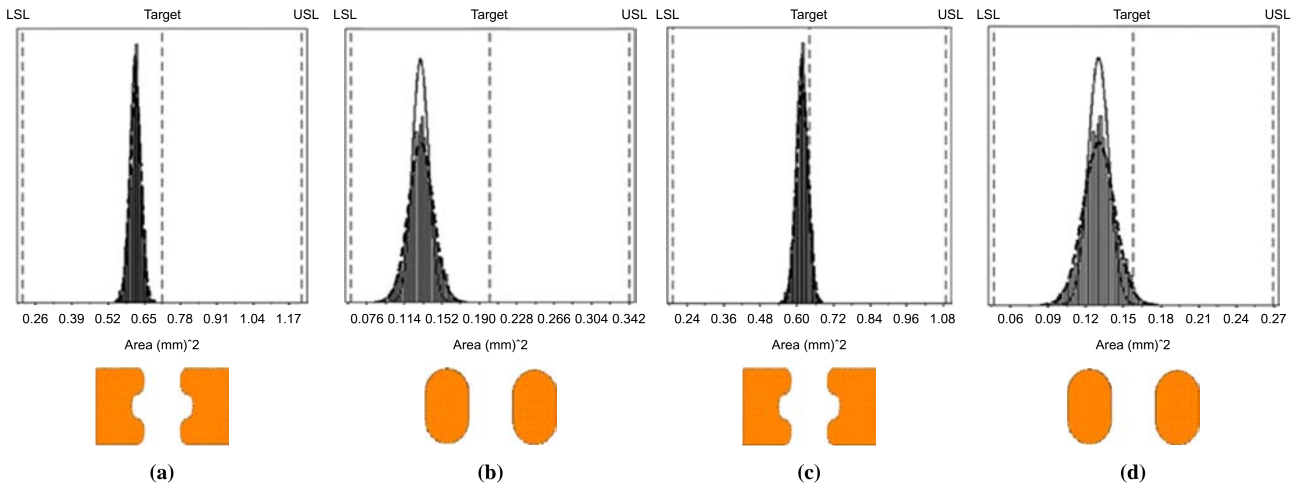
$$Ca = \frac{|((USL + LSL)/2) - \hat{\mu}|}{(USL - LSL)/2} \qquad (1)$$

where USL is the upper specification limit, LSL is the lower specification limit and $\hat{\mu}$ is the estimated average.

5.2 Establish SPI specification based on the CoPQ

As mentioned earlier, a total of 47 bonding pads were found to have solder shorts. The majority of these defective samples were fine-pitch leaded components. In this section, a TSOP with 0.4-mm pitch has been used to determine the desired SPI specification (USL). It is assumed that the cost of a "false alarm" is $1. A "false alarm" is defined as a non-defective sample rejected during the SPI stage and washed/re-printed. This involves manpower and material expenses

Figure 19 Distributions of solder area depositions on (a) and (c) concave and (b) and (d) oval pads before and after adjustments of specification nominal



during the repairing process. It has also been assumed that the cost of an "escaped" sample is $2. An "escaped" sample is defined as a sample with excessive solder volume deposition but not rejected during the SPI stage, in which a solder short is detected at the AOI stage and therefore needs to be de-soldered/repaired after the reflow soldering process. In additional to the above-mentioned repair expenses, the de-soldering process also involves the risk of damage to the bonding pad. The USL may then be determined by minimizing the total cost.

Figure 20 shows the distributions of solder volume (in mm^3) depositions on the pads with and without shorts. The amount of solder deposition follows a normal distribution; the occurrence of samples with more excessive solder volume was less frequent. The samples were categorized based on the solder volume deposition (equation (2)). This helped to show the correlation between the solder volume and probability of the occurrence of solder shorts. Table VIII displays the set boundaries of each class, the number of samples with and without shorts and the probability of occurrence in defective parts per million (DPPM). Data from the first three classes exhibited no shorts and were therefore removed from further calculation. The remaining data were assumed to follow a Weibull distribution (equation (3)). The accumulative probability functions of each class were calculated and used to determine the parameters of the Weibull distribution, shape parameter β and scale parameter θ.

For the data with shorts, β and θ were 8.197 and 0.05451, respectively. For data without shorts, β and θ were 7.370 and 0.04856, respectively. The assumption that the data follow a Weibull distribution was then verified through the K-S hypothesis test at a confidence level of 0.05. The probabilities of escapes and false alarms with solder depositions in the range of 0.035-0.060 mm^3 were calculated based on the pre-determined Weibull distribution (Table IX). The total CoPQ can therefore be determined using equation (4).

Figure 20 Distributions of solder volume depositions with and without shorts

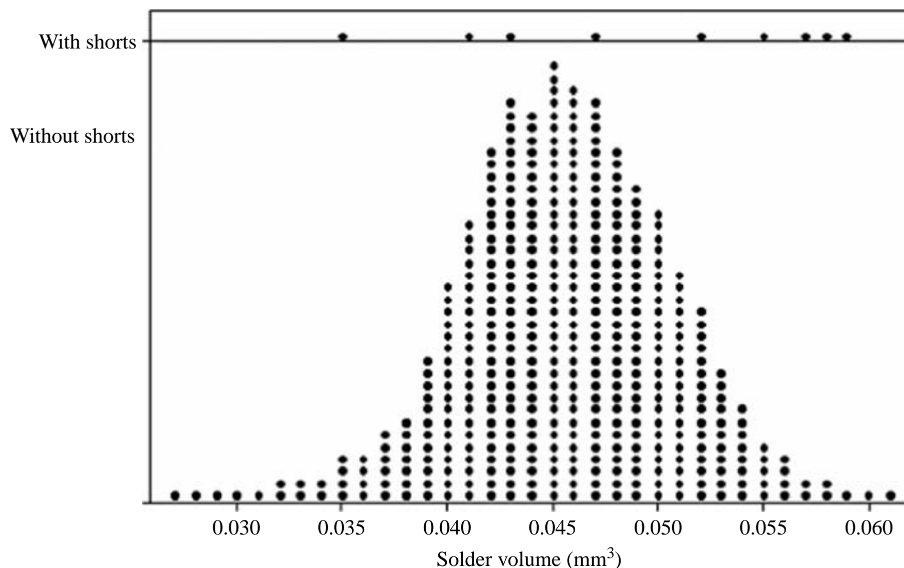


Table VIII Number of samples in each class and the DPPM

Class	Class midpoint (mm^3)	Lower boundary (mm^3)	Upper boundary (mm^3)	No. w/short	No. w/o short	Short DPPM	W/o short PPM
1	0.035	0.034	0.037	1	277	3,597	996,403
2	0.038	0.037	0.039	0	386	0	1,000,000
3	0.040	0.039	0.042	2	1,464	1,364	998,636
4	0.043	0.042	0.044	0	1,612	0	1,000,000
5	0.045	0.044	0.047	1	2,537	394	999,606
6	0.048	0.047	0.049	2	1,458	1,370	998,630
7	0.050	0.049	0.052	1	1,541	649	999,351
8	0.053	0.052	0.054	1	552	1,808	998,192
9	0.055	0.054	0.057	2	318	6,250	993,750
10	0.058	0.057	0.059	2	62	31,250	968,750
11	0.060	0.059	0.062	0	18	0	1,000,000

Table IX Probability of escape and false alarm with varying solder deposition and the resulting CoPQ

Solder volume (mm^3)	Probability of escape	Escape cost	Probability of false alarm	False alarm cost	Expected total cost
0.035	0.02615	0.05230	0.91435	0.91435	0.96664
0.036	0.03283	0.06565	0.89565	0.89565	0.96130
0.037	0.04092	0.08184	0.87383	0.87383	0.95568
0.038	0.05066	0.10133	0.84861	0.84861	0.94993
0.039	0.06230	0.12461	0.81972	0.81972	0.94432
0.040	0.07611	0.15222	0.78696	0.78696	0.93919
0.041	0.09237	0.18475	0.75022	0.75022	0.93497
0.042	0.11138	0.22277	0.70947	0.70947	0.93224
0.043	0.13343	0.26686	0.66482	0.66482	0.93168
0.044	0.15879	0.31757	0.61655	0.61655	0.93412
0.045	0.18770	0.37539	0.56512	0.56512	0.94051
0.046	0.22036	0.44071	0.51116	0.51116	0.95187
0.047	0.25688	0.51377	0.45551	0.45551	0.96928
0.048	0.29730	0.59460	0.39919	0.39919	0.99379
0.049	0.34150	0.68300	0.34334	0.34334	1.02635
0.050	0.38923	0.77846	0.28920	0.28920	1.06766
0.051	0.44006	0.88012	0.23797	0.23797	1.11809
0.052	0.49337	0.98675	0.19081	0.19081	1.17756
0.053	0.54837	1.09674	0.14866	0.14866	1.24539
0.054	0.60406	1.20813	0.11218	0.11218	1.32031
0.055	0.65934	1.31869	0.08172	0.08172	1.40041
0.056	0.71300	1.42600	0.05726	0.05726	1.48326
0.057	0.76382	1.52764	0.03844	0.03844	1.56609
0.058	0.81067	1.62135	0.02462	0.02462	1.64597
0.059	0.85260	1.70520	0.01497	0.01497	1.72018
0.060	0.88891	1.77782	0.00860	0.00860	1.78642

While the cost of escape and the cost of false alarm and the resulting CoPQ are functions of the USL during the SPI stage, the desired specification can be established by minimizing the total CoPQ. As a result, USL of 0.043 mm^3 is suggested for the 0.4-mm pitch TSOP, corresponding to a minimum total cost of \$0.9317 (Table IX):

$$N_c = 1 + 3.33 \times \log\ n \tag{2}$$

where N_c is the number of classes and n is the total number of solder joints:

$$f(x) = 1 - \exp\left[-\left(\frac{x}{\theta}\right)^{\beta}\right] \tag{3}$$

where F(x) is the function of a Weibull distribution, x indicates the amount of solder deposition, θ is the scale parameter and β is the shape parameter:

$$CoPQ = P_e \times C_e + P_f \times C_f \tag{4}$$

where CoPQ is the total CoPQ and P_e and P_f are the probabilities of escape and false alarm, respectively. C_e and C_f are the costs of escape and false alarm, respectively.

6. Conclusions

First, this study has provided a comprehensive review of critical parameters in the solder paste printing process. The key findings are:

- the higher the printing pressure, the more solder paste is scooped away, leading to lower solder deposition;
- there is a significant difference in solder deposition between the front squeegee and the rear squeegee due to the configurations of the fixtures;
- insufficient distance between the stencil aperture and the initial printing location results in irregular solder paste and variation in solder deposition;
- a stencil with a higher area ratio results in greater solder deposition and less variation; and
- stencil apertures parallel to the direction of printing are superior to a 45° vector print.

Second, the correlation between the results of SPI analysis and post-reflow defective scenarios has been examined. The majority of tombstones and opens observed in this case study was not due to inappropriate solder volume. Shorts were found to indeed relate to excessive solder deposition. In this study, shorts accounted for 70 per cent of all defects. This observation is consistent with the literature, where approximately 60-70 per cent of soldering defects are attributed to the solder paste printing process.

Finally, SPI specifications are suggested. Considering the thicknesses of the solder mask and the legend ink, the nominal solder thickness should be the stencil thickness $+0.038$ mm. Further, there is an offset in the results of SPI measurements between the SMD pads and NSMD pads. The nominal solder thickness of SPI specifications should take this offset into consideration. In addition, due to the limitation of template frames used for the SPI apparatus, the specifications for solder deposition with irregular stencil apertures need to be adjusted. Lastly, considering the cost of an escaped sample, the cost of a false alarm and the corresponding probabilities of occurrence, the USL has been established by minimizing the total cost.

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